1 – 16 (Deleted)

17. (Original) A programmable macro look up table (macro-LUT) circuit for an integrated circuit, comprising:

a plurality of LUT circuits, each of said LUT circuits comprising a LUT output, at least one LUT input, and at least two LUT values; and

a programmable means of selecting LUT inputs to at least one of said LUT circuits from one or more other LUT circuit outputs and external inputs, and selecting LUT values to at least one of said LUT circuits from one or more other LUT circuit outputs and configurable logic states, said programmable means further comprised of two selectable manufacturing configurations, wherein:

in a first selectable configuration, a random access memory circuit (RAM) is formed, said memory circuit further comprising configurable thin-film memory elements;

in a second selectable configuration, a hard-wire read only memory circuit (ROM) is formed in lieu of said RAM, said ROM duplicating one RAM pattern in the first selectable option.

18. (Original) The circuit of claim 17, further comprising one or more registers to latch data from one or more of said LUT outputs.

19. (Original) The circuit of claim 17, wherein said RAM element is selected from one of fuse links, anti-fuse capacitors, SRAM cells, DRAM cells, metal optional links, EPROM cells, EEPROM cells, flash cells, ferro-electric elements, optical elements, electro-chemical elements

and magnetic elements.

20. (Original) The circuit of claim 17, further comprising a macro LUT response time characteristic, said response time comprising a transit time of a LUT value to a macro LUT output, wherein said response time is substantially identical between the two selectable manufacturing configurations.